“Ghosts in the machine – how subatomic-scale events impact us and what we can do about it”

by

Robert C. Baumann

IEEE and Texas Instruments Fellow
Texas Instruments, Dallas, Texas, USA
Outline

• Introduction
• Terrestrial Radiation Sources
• Technology Sensitivity Trends
• Derating – not all fails are equal
• Mitigation Strategies
• Summary
Definitions

**Hard Error**

An error induced by faulty device operation. DATA is lost AND data can no longer be stored at that location.

**Soft Error**

A random error induced by an event which corrupts the DATA stored in a device. The device itself is not damaged.

**Soft Error Rate (SER)**

- Electromagnetic Interference (EMI)
- Circuit-level electrical noise
- Board-Level electrical noise
- Process Variability + Marginality
- Ionizing Radiation
  - Random in time and location
  - Dominant “noise” in well designed systems
  - Terrestrial => alpha particles + cosmic rays
More Definitions!

SEE

- Single event effects

SET

- Single event transient

SEFI

- Single event latch-up

SEGR/SEB

- Single event gate rupture/Burnout

MBU

- Single event func. interrupt

SBU

- Single bit upset

SEU

- Single event upset

SEL

- Single event func. interrupt

Soft Error

Hard Error
Motivation – Why do we care…

◆ Soft errors induce the highest failure rate of all other reliability mechanisms combined.

◆ Soft errors impact customer perception of reliability. Undetected errors are viewed as the biggest threat since their impact on applications cannot be predicted.

◆ The problem gets worse as circuit densities are increased and voltages are decreased. Many design tweaks for low power often make soft error susceptibility much worse!
Extrinsic Failures (ppm)  Intrinsic Failures (FIT)  Wearout (lifetime)

Bathtub Curve

Time
Useful Life

In a qualified product, radiation effects are a time-zero quality issue while hard failures are typically related to wear-out phenomena.
Reverse-biased N+/P junction

Ions (alphas, protons, secondary products from neutron reactions) and electrons generate localized, transient charge clouds that are collected and dissipated by drift, diffusion, and recombination.
mysterious glitch has been popping up since late last year...It has caused problems for America Online, Ebay and dozens of other major corporate accounts...The Sun has caused crashes at dozens of customer sites.

An odd problem involving stray cosmic rays and memory chips in the flagship Enterprise server line...Sun found it had been shipping servers whose cache modules contained faulty SRAM chips from a supplier it won't name.

Loss of customer confidence = Loss of revenue
~ $1 Billion
Toyota Sudden Acceleration: The Story Unfolds

...engineers...demonstrate that problems can exist in which Toyota’s Electronic Control Unit (ECU) doesn’t detect a critical system failure...once the redundant signal is lost and undetected as an error, the vehicle is in an unsafe condition ...SEU is one possible explanation for sudden unintended acceleration (SUA) in Toyotas.

(from The Safety Record, Volume 7, Issue 1, April 2010)

Toyota faces numerous personal injury and wrongful death lawsuits in federal courts due to their defective vehicles. The value of claims ... about $4 billion

Zacks Equity Research, On Friday August 27, 2010

Loss of customer confidence
(+ loss of customers!)

= Loss of revenue

> $4 Billion
Cosmic Radiation is out there!

Galactic Particles (E >> 1 GeV)
Solar Wind (usually E < 1 GeV)

- 92% Protons
- 6% Alpha Particles (He)
- 2% γ and heavy ions

courtesy of Marvel Comics
"Fantastic Four" issue #1

courtesy of NASA shuttle homepage
Cosmic Cascade

Single Incoming Cosmic Particle

Ground flux of electrons, muons, neutrons, and protons.
Cosmic Rays on the Ground


~ 13 n/cm²-hr
@ sea-level, NYC
Eₙ ≥ 10 MeV
Terrestrial Environment


- $^{25}\text{Mg} + \alpha$ 2.75 MeV
- $^{28}\text{Al} + p$ 4.00 MeV
- $^{27}\text{Al} + d$ 9.70 MeV
- $^{24}\text{Mg} + n + \alpha$ 10.34 MeV
- $^{27}\text{Al} + n + p$ 12.00 MeV
- $^{26}\text{Mg} + ^3\text{He}$ 12.58 MeV
- $^{21}\text{Ne} + 2\alpha$ 12.99 MeV

Other reactions may also contribute significantly, e.g. n + O, n + Cu, etc. n + W,
Altitude Dependence


Going from 0 to 10,000 feet corresponds to a relative neutron flux range of 1.0 to 11.4x.

<table>
<thead>
<tr>
<th>Altitude (feet)</th>
<th>Relative Flux</th>
<th>% Urban</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1.0</td>
<td>35%</td>
</tr>
<tr>
<td>1200</td>
<td>1.5</td>
<td>80%</td>
</tr>
<tr>
<td>1700</td>
<td>1.7</td>
<td>90%</td>
</tr>
<tr>
<td>3600</td>
<td>2.4</td>
<td>95%</td>
</tr>
<tr>
<td>5000</td>
<td>2.9</td>
<td>99%</td>
</tr>
<tr>
<td>10000</td>
<td>11.4</td>
<td>&gt;99.99%</td>
</tr>
</tbody>
</table>

Pop. data from public World Bank and CIA Databases.
Latitude Dependence


A computer simulation of Earth's magnetic field structure

Extinction by Cosmic Rays?


with permission from artist by Joe Tucciarone “Cryolophosaurus” http://members.aol.com/Dinoplanet/cryo.html
Solar Cycle Dependence

Solar eruptions follow the "11-year sun-spot cycle"

Average variation in neutron flux < 15%
Max. Variation in neutron flux < 30%

Solar events can either increase OR decrease the terrestrial flux!

Photo courtesy of NASA

Moscow Neutron Monitor - http://cr0.izmiran.rssi.ru./mosc/main.htm

Relative Neutron Count


Time
High Energy = Multiple Bit Upsets

Typical 65nm SRAM $Q_{\text{crit}}$

Larger clusters of errors are typically from high energy neutron reactions

Accelerated Neutron Testing

neutron test procedure in JESD89 and JESD89A

Close match between terrestrial background spectrum and Los Alamos means extrapolation is based on a simple multiplication
Alpha Particles

From radioactive decay of impurities

\[
\text{d}Q/\text{d}x \ (\text{fC/\mu m})
\]

\[
\text{Range } \ (\text{\mu m})
\]

\[
\begin{align*}
\text{Particle Energy } & (\text{MeV}) \\
0 & 5 \\
10 & 15 \\
20 & 25 \\
\end{align*}
\]

\[
\begin{align*}
\text{Intensity } & (\text{arbitrary units}) \\
0 & 20 \\
40 & 60 \\
80 & 100 \\
\end{align*}
\]

\[
\begin{align*}
238\text{U} \\
232\text{Th}
\end{align*}
\]
What the Chip “Sees”

- **Standard**: $10 - 0.01 \, \alpha/\text{cm}^2\text{-hr}$
- **Low Alpha**: $< 0.01$
- **Ultra Low Alpha**: $< 0.002$
- **Hyper Low Alpha**: $< 0.0005$

**α from packaging materials dominate.**

$< 0.002 \alpha/\text{cm}^2\text{-hr}$ implies $< 100 \text{ p.p. TRILLION!}$

### Sample Description Table

<table>
<thead>
<tr>
<th>Sample Description</th>
<th>Detector</th>
<th>CDL95</th>
<th>MDA95</th>
<th>average</th>
<th>conf.</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECD Cu 10um</td>
<td>4950</td>
<td>0.00019</td>
<td>0.00054</td>
<td>0.00036</td>
<td>91.47%</td>
</tr>
<tr>
<td>Barrier Layer</td>
<td>4950</td>
<td>0.00012</td>
<td>0.00033</td>
<td>0.00000</td>
<td>-</td>
</tr>
<tr>
<td>Interlevel Dielectric</td>
<td>4950</td>
<td>0.00012</td>
<td>0.00035</td>
<td>0.00039</td>
<td>99.96%</td>
</tr>
<tr>
<td>Interlevel dielectric</td>
<td>4950</td>
<td>0.00013</td>
<td>0.00036</td>
<td>0.00027</td>
<td>93.41%</td>
</tr>
<tr>
<td>Alternate dielectric</td>
<td>4950</td>
<td>0.00012</td>
<td>0.00034</td>
<td>0.00011</td>
<td>-</td>
</tr>
<tr>
<td>diborane based W process</td>
<td>4950</td>
<td>0.00012</td>
<td>0.00034</td>
<td>0.00007</td>
<td>-</td>
</tr>
<tr>
<td>Bare silicon wafers</td>
<td>4950</td>
<td>0.00012</td>
<td>0.00034</td>
<td>0.00004</td>
<td>-</td>
</tr>
<tr>
<td>Full process 8LM Cu wafer</td>
<td>4950</td>
<td>0.00013</td>
<td>0.00037</td>
<td>0.00028</td>
<td>93.78%</td>
</tr>
<tr>
<td>Full process 8LM Cu wafer 2</td>
<td>4950</td>
<td>0.00013</td>
<td>0.00072</td>
<td>0.00018</td>
<td>62.74%</td>
</tr>
</tbody>
</table>

**Units in $\alpha/\text{cm}^2\text{-hr}$**

- **Standard**: 10 - 0.01 $\alpha/\text{cm}^2\text{-hr}$
- **Low Alpha**: $< 0.01$
- **Ultra Low Alpha**: $< 0.002$
- **Hyper Low Alpha**: $< 0.0005$

---

- **measured 232-Th Foil**: 
- **pkg/chip sim. emission**: 

---

**Intensity (arbitrary units)**

**Alpha Energy (MeV)**

- **measured 232-Th Foil**
- **pkg/chip sim. emission**

---

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Accelerated $\alpha$-Particle Testing

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<tr>
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<th>conf.</th>
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<td>0.00019</td>
<td>0.00054</td>
<td>0.00036</td>
<td>91.47%</td>
</tr>
<tr>
<td>90nm Barrier Layer</td>
<td>0.00012</td>
<td>0.00033</td>
<td>0.00000</td>
<td>-</td>
</tr>
<tr>
<td>90nm Interlevel Dielectric</td>
<td>0.00012</td>
<td>0.00035</td>
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<td>0.00027</td>
<td>96.41%</td>
</tr>
<tr>
<td>65nm Alternate dielectric</td>
<td>0.00012</td>
<td>0.00034</td>
<td>0.00011</td>
<td>-</td>
</tr>
<tr>
<td>diborane based W process</td>
<td>0.00012</td>
<td>0.00034</td>
<td>0.00007</td>
<td>-</td>
</tr>
<tr>
<td>Bare silicon wafers (90nm)</td>
<td>0.00012</td>
<td>0.00034</td>
<td>0.00004</td>
<td>-</td>
</tr>
<tr>
<td>Full process BLM Cu wafer</td>
<td>0.00013</td>
<td>0.00037</td>
<td>0.00028</td>
<td>96.78%</td>
</tr>
<tr>
<td>Full process BLM Cu wafer 2</td>
<td>0.00013</td>
<td>0.00072</td>
<td>0.00018</td>
<td>62.74%</td>
</tr>
</tbody>
</table>

$\alpha$-Counting materials database

**TI $\alpha$Shield** code calculates actual alpha particle flux ($\alpha$/hr) reaching the Si

**TI RadLabXP Code**

Alpha Sensitivity (errors/$\alpha$)

Fail rate due to alpha particles

accelerated $\alpha$ASER Test
$^{10}\text{B}$ and Thermal Neutrons

90% of all $^{10}\text{B}$ fissions are induced by neutron energies below 15 eV!

Recently TSMC reported a 10% effect from metal plug process using borane.
Key Terrestrial Mechanisms

**Alpha Particles**

**High Energy Neutrons**
$n (> 1 \text{ MeV})$
$^{28}\text{Si, }^{16}\text{O, etc.}$

**Thermal Neutrons**
R.C. Baumann et al., IEEE IRPS, p. 299, 1995

$n (< 100 \text{ eV})$


Recently:
- Muons?
- Protons?
- electrons?
Future Terrestrial Mechanisms?

If these simulations are correct, when $Q_{\text{crit}}$ reaches 0.2 fC SER will double from muons alone and at 0.1 fC SER will be 5-10x higher. Note: current 40nm technologies have a $Q_{\text{crit}}$ in the 0.6 – 1.2 fC range.

Terrestrial Proton may also contribute as $Q_{\text{crit}}$ is reduced due to the much higher cross-section for direct ionization.

DRAM better than SRAM


< 5% of SER is due to failures in DRAM in modern systems (assuming 1000x more DRAM is used)

Note this is external DRAM

DRAM is $10^4$ times less sensitive than SRAM
SRAM bit SER Trends

High Density cell, 25C, ULA wirebond, sea-level, data (points) at nominal core voltage, 7LM for c035-c014 and 5LM for c10-c05.

Sigma is NOT variation but SER at \( V_{\text{min}} \) -10% and \( V_{\text{max}} \) +10%

Charge scaling regime

Area scaling dominated regime

\[
\text{SER} \propto \text{Area}
\]

Technology (nm)

<table>
<thead>
<tr>
<th>Technology</th>
<th>V_nominal</th>
<th>V_core</th>
</tr>
</thead>
<tbody>
<tr>
<td>C10</td>
<td>350nm</td>
<td>3.3V</td>
</tr>
<tr>
<td>C07</td>
<td>250nm</td>
<td>1.8V</td>
</tr>
<tr>
<td>C05</td>
<td>180nm</td>
<td>1.5V</td>
</tr>
<tr>
<td>C035</td>
<td>130nm</td>
<td>1.2V</td>
</tr>
<tr>
<td>C027</td>
<td>90nm</td>
<td>1.1V</td>
</tr>
<tr>
<td>C021</td>
<td>65nm</td>
<td>1.1V</td>
</tr>
<tr>
<td>C014</td>
<td>40/45nm</td>
<td>1.0V</td>
</tr>
<tr>
<td>C28</td>
<td>28nm</td>
<td>0.9V</td>
</tr>
</tbody>
</table>

TI leads industry by removing BPSG.
Chip-Level SRAM SER Trends

Chip integration levels determined from high performance DSP and ASIC products

General Trend
More bits = Higher SER

Technology (nm)
Neutron SER curves are modified by geographical location (these are sea-level NYC as per JEDEC JESD89A). These curves are generated for room temperature.

Alpha SER curves are modified by package type and number of metal layers and final SER estimates will be lower than that in these curves. These curves are generated for room temperature and assume a Si surface alpha flux of 0.002 a/cm²-hr.
Why Care About Logic SER?

**Derated Logic SER**
(15% - 5%)

**Assumptions:**
- FF/Latch SER ~ SRAM bit SER
- A product with 24Mbit HD SRAM
- Flop instances = 10% of SRAM
- Logic de-rating 15% - 5%
- ULA wire-bond, sea-level, 6LM, 25°C
  - C05 @ 1.5V, C035 @ 1.3V, C027 @ 1.2V
  - C021 @ 1.1V, C014 @ 1.1V

**Business Zones**
- Hand-held
- Single comp. consumer
- System w multiple units
  - Higher Rel expectations
- Auto, Medical
  - Safety
  - High rel. expectations

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Sequential Logic

45nm Logic Test Chip
nSER @ 0.84V

HP SRAM nSER ~ 570 Fit/Mbit

Chain 1 = lowest $Q_{crit}$
Chain 2 = median $Q_{crit}$
Chain 3 = most used flop
Chain 5 = high drive Flop
Chain 6 = min drive Flop
Chain 7 = HVT version of #3
Chain 4,8 = DICE (rad-hard flop)

nSER of rad-hard DICE Flop is ~ 80x lower than average for standard flops
Combinatorial Logic

Event + propagation + timing => SEU in register

\[ P_{\text{tran}}(t) \times P_{\text{prop}}(t) \times P_{\text{capt}}(t) = ? \]

Transistor

Detected by event prob. + circuit susc.

Transient

Use of gated clocks
Reduces this

Transient propagation

Analog filtering no longer applies – typical pulses are easily propagated

Combinatorial Logic

Output Effected?
SET – a dominant problem?


Logic SER increased < 5% from SET at maximum operating frequency

For speed, the depth of combinatorial logic and hence its probability of it being upset has been decreasing with scaling,
What Can We Do?

Is the sky really Falling?

Does each soft error REALLY lead to a product failure?
What is Derating?

SEE derating factor = \( \frac{\text{Machine Fails}}{\text{Total Soft Fails}} \)

Ranges from 1 to 0

Hang Nguyen and Yoad Yagil, 2003
IEEE IRPS presentation

Memory (SRAM, Register Arrays, CAM)

Combinatorial Logic

Sequential Logic
Memory Derating

<table>
<thead>
<tr>
<th>Instruction Cache RAM</th>
<th>Effect Fail</th>
<th>&quot;location&quot;</th>
<th>Fail %</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0.0000%</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>1</td>
<td>6.6667%</td>
<td></td>
</tr>
<tr>
<td>92</td>
<td>1</td>
<td>30.6667%</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>37.3333%</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MEMC</th>
<th>Effect Fail</th>
<th>&quot;location&quot;</th>
<th>Fail %</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>3</td>
<td>0.0000%</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0.2857%</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>1.5714%</td>
<td></td>
</tr>
<tr>
<td>56</td>
<td>1</td>
<td>8.0000%</td>
<td></td>
</tr>
<tr>
<td>68</td>
<td>1</td>
<td>9.7143%</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>19.5714%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Memory derating example from SUN picoJAVA-II uP adapted from S. Kim and A. Somani, IEEE Proc. Internat. Conf. on Dependable Systems and Networks (DSN’02), 2002.

In this case only 37% of fails in the Cache led to machine fails thus 63% of soft errors had no effect on reliability.
Data Sensitivity Effect

MSB

LSB
Circuit-Level Derating

Logical Masking

Electrical Masking

Latching Window Masking
(Timing Derating)

Clock
D(t₁)
D(t₂)
D(t₃)
D(t₄)

Glitch is Captured
Logic Derating Examples


Chip Multiprocessor (CMP) interconnection network switch. Simple chip but has same features as CPU flow.

Only ~ 3% of fails in logic caused a failure in the switch fabric ASIC under high utilization benchmark.

7% of soft errors in logic caused a failure in the CPU.

Abatement strategies

Let’s assume we derate all components and soft failure rates are still too high – what can we do?

Process/Layout Level

- Mitigation of sources (alpha particles, $^{10}\text{B}$)
- Process technology tweaks (doping, SOI)
- Component Layout ($A_{junc}$, $C_{gate}$, $I_{drive}$, $V_c$)

Block Level

- Parity/ECC on Memory (MUX factors/Coverage)
- Hardened Logic (Node redundant, isolation wells)
- TMR (redundancy with hardened voting)

Architecture/System/Software Level

- Processor Redundancy (lock step)
- Process Redundancy (watchdogs, instruction checks, etc.)
Substrate Impact

Deep tank/Buried implants

- Reduce prompt charge collection by reducing funnel.
- Reduce collected charge by allowing more efficient substrate collection of diffusing carriers

Multiple Well Technology

- Drain/well and source/well fields reduced thus charge collection is reduced.
- Charge collected by buried well and substrate can be removed.
- Charge sharing by source/well depletion reduces charge collected by drain node.
- Good at eliminating SEL but due to its depth it does not reduce SEU significantly

< 3x improvement
Substrate Impact - Strain

from N. Mahatme, B. Bhuva, Y. Fang, and A. Oates, “Impact of Strained-Si PMOS Transistors on SRAM Soft Error Rates”, IEEE RADECS, Seville, Spain, September 2011
SOI vs. Bulk

SOI reduces SER by 4x – 10x

4x - 6x SER reduction

SOI reduces SER by 4x – 10x

Other Memory Technologies


**“Simple” Error Detection & Correction**

- Assume probability of multiple bits within a word is zero
- Store two additional copies of the data word
- On read out, compare three words and check for match
- If one word does not match then use the other two in a majority voting scheme to reset the bits in the word that does not match
- Cost for “Simple ECC” = 3x area/power + voting logic

The goal of coding is to use “smart” encoding that achieves the same error correcting capability but much more efficiently.

**Parity**

Add one bit - detect single errors

(Generated by XOR)

**3-Repetition Code**

Triple bits - correct single errors

---

From “Error-Correcting Codes”, G. Eric Moorhouse,
http://math.uwyo.edu/~moorhous/quantum/
Information Distance, $d=3$

A single bit error anywhere in our 5 bit CODE word generates one of 5 possible UNIQUE vectors.

A double bit error generates one of 10 possible error vectors (that are not UNIQUE in $d=3$).

Thus any single error coding scheme must ensure the valid code words are “far enough apart” in information space that single bit flips create vectors that:

1.) Do not represent other valid code words (error detectable)
2.) Uniquely identify the original code word (error correctable)
3.) By extension this means that the minimum hamming distance for such a system must be $d=3$
**Single and Double Bit Errors**

*Words* encoded so Hamming distance between two unique words is \( d \geq 3 \).

A single bit error leads (single arrow) to a vector which is uniquely identified and thus CORRECTABLE. A double error is DETECTABLE since it is not transformed into another valid data word, however it is no longer unique and thus is NOT CORRECTABLE. One can design a \( d>3 \) code, effectively putting greater “distance” between code words BUT code efficiency drops FAST! (\( d=4 \) requires 2x the area).

Note that \( d=2 \) and \( d=3 \) errors are shown as a sum of single bit errors for clarity - in an actual SER scenario the multi-bit errors occur as a single event.
ECC Implementations


Properly Implemented, ECC reduces memory SER By 1000 – > 10,000x


<table>
<thead>
<tr>
<th>Data Bits</th>
<th>SEC-DED</th>
<th>SBC-DBD (B=4 bits)</th>
<th>DEC-TED</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>check bits</td>
<td>overhead</td>
<td>Total Bits</td>
</tr>
<tr>
<td>16</td>
<td>6</td>
<td>38%</td>
<td>22</td>
</tr>
<tr>
<td>32</td>
<td>7</td>
<td>22%</td>
<td>39</td>
</tr>
<tr>
<td>64</td>
<td>8</td>
<td>13%</td>
<td>72</td>
</tr>
<tr>
<td>128</td>
<td>9</td>
<td>7%</td>
<td>137</td>
</tr>
</tbody>
</table>

Straight memory layout overhead - on a per chip area the overhead will be much smaller
Impact of Memory Organization

5 bit error
1 triple bit error (not detected) &
1 double error that is detectable but NOT correctable

5 bit error
1 double error that is detectable but NOT correctable
3 single bit errors that are all correctable.

Proper interleaving is critical < 8% of errors are MBU
State Redundancy Hardening

Dual Interlocked Storage Cell (DICE): Does not upset unless two common nodes are upset

DICE cost ~ 2x the layout* ~ 2x the power


Fig. 3. Principle of the dual interlocked storage cell

nSER of properly implemented DICE Flops is 20 – 100x lower than conventional flops and $\alpha$SER ~ 200 - 1000x lower.

Fig. 17. D Flip-Flop cross-section, upset threshold is well within the LET range for alpha particles and neutron generated particles [19].
Full Processor Redundancy

NOTE! When error discovered the circuit that deal with putting the system in a safe-mode must be hardened. Likewise the voter in TMR systems must be hardened.
Efficacy Summary

Process Level

- Mitigation of sources (alpha particles, $^{10}$B) 2x – 50x
- Process technology tweaks (doping, SOI) 1.5x – 10x
- Component Layout ($A_{junc}$, $C_{gate}$, $I_{drive}$, $V_c$) 1.5x – 3x (150*x)

Block Level

- Parity/ECC on Memory > 1000x
- Hardened Logic > 50x
- TMR > 1000x

Architecture/System/Software Level

- Processor Redundancy (lock step) > 1000x
- Process Redundancy (watchdogs, etc.) > 100x
- Software Redundancy (threads, etc.) > 10x - 100x*
Closing Remarks

- As critical charge is scaled down sensitivity to ionizing radiation has been decreasing slightly with each recent generation BUT other mechanisms may cause dis-continuously high SER at very low $Q_{\text{crit}}$ (muons, protons). Higher bit density always leads to higher SER.

- Use of ECC will be ubiquitous for SOCs w large memories. However, SER is application-specific so a single failure rate specification for all products does not work.

- Hardened logic or architectural-level checking will become more widespread since sequential logic sensitivity now exceeds that of SRAM on a per bit (flop) basis.

- New nano-devices may offer improved resilience against SEE (FinFET, carbon nanotube, etc.) but will not eliminate them and these devices may be more susceptible to dose effects.

- Vendors that ignore the soft error problem will end up paying for it in loss of customer confidence – leading to significant revenue loss.