From COTS to Space-Grade Electronics: Which is best for your mission?

Sponsored in part by Texas Instruments HiREL

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Spoiler alert! It depends on the mission!
Short Course Outline

- Space Environment Challenges
- “New Space” vs. Traditional Space
- What’s in a Name?...Semiconductor Grades
- Quality, Reliability, and the Bathtub Curve
- Microelectronics Manufacturing Variation
- Radiation Effects Sensitivity to that Variation
- Up-screening vs. Higher Grade – PROs and CONs
- Summary
Space…A Harsh Mistress

Mechanical
- Vibration
- Vacuum/Outgassing
- Stress cycling (thermally induced)

Chemical
- Out-gassing (vacuum) - plastics?
- Metal bond robustness (Cu, Au, vs. Al)
- TIN whiskers

Large Temperature Ranges (-55° to 125°C)

Magnetic fields, EMC, Charging effects, Zero-G…

High Radiation Environment => TID, DDD, SEE

Quality & Reliability
- Time-zero Quality & Early Failures
- Process variation = variation in Rad. sensitivity
Commercial-Off-The-Shelf (COTS) Grades

“To meet future needs, the Department of Defense must increase access to commercial state-of-the-art technology and must facilitate the adoption by its suppliers of business processes characteristic of world class suppliers…”

1994 Policy Memo, Dr. William Perry, Secretary of Defense

**COTS:** An assembly/part designed for commercial applications for which the item manufacturer or vendor solely establishes and controls the specifications for performance, configuration, and reliability. For example, any catalog assembly or part received “as-is” without any additional testing after delivery.

**COTS+:** A COTS part + additional test data establishing random failure rate assumptions, performance consistent with the manufacturers data sheet and methods to exclude early failing parts, parts with latent defects, weak parts, or counterfeit parts. For example, AEC-certified or compliant automotive parts.

Adapted from Reference NASA/TM-2014-218261
COTS Radiation-Hardened by “Serendipity”

“One Size” does NOT fit all

“Traditional” SPACE
QMLV, ceramic, GEO, LEO, etc.
mission life: decades
“Failure is NOT an option”

“New” SPACE
Predominantly LEO, plastic is OK,
Lower criticality
Duration: ~ a few years
Small Sats: A big part of “New Space”

Small sats launch costs are lower = budget for electronics is tighter than larger missions - since potential volume is higher, these are the primary target for intermediate-grades.

Grades…What’s in a Name?

COTS

COTS+

?  

QMLQ

QMLV, RHA Space-grade

- Enhanced Product (EP), Aerospace Qual. (AQEC) ADI
- Radiation-Tolerant Plastic (ISL71xxxM) Renesas (Intersil)
- Ruggedized Plastic (PR3, PR2, PR1) Maxim
- Ruggedized Plastic (RobuST) ST Micro
- Enhanced Plastic, Space EP (EP, SEP) TI

This list is neither complete nor comprehensive, it merely is included to show that multiple vendors offer intermediate-grades – I apologize in advance for anyone that was left out!
### Product Grades “Decoder Ring”

#### Quality / Reliability

<table>
<thead>
<tr>
<th></th>
<th>COTS / COTS+</th>
<th>Enhanced Intermediate Grades</th>
<th>Space Grade</th>
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<tbody>
<tr>
<td></td>
<td>Commercial</td>
<td>AEC-Q100</td>
<td>EP</td>
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<td></td>
<td></td>
<td>QMLQ</td>
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<td></td>
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<td>Space EP</td>
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<td>QML-V</td>
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<td>NO</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
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<tr>
<td>Bond wires</td>
<td>Au or Cu</td>
<td>Au or Cu</td>
<td>Au</td>
<td>AI</td>
<td>Au</td>
<td>AI</td>
<td>AI</td>
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<tr>
<td>Pure Sn Used</td>
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<td>Burn-in Performed</td>
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<td>NO</td>
<td>NO</td>
<td>NO</td>
<td>NO</td>
<td>YES</td>
<td>YES</td>
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<td>Radiation Tested</td>
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<td>YES</td>
<td>YES</td>
<td>YES</td>
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<td>Radiation Assured</td>
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<td>NO</td>
<td>NO</td>
<td>NO</td>
<td>YES</td>
<td>NO</td>
<td>YES</td>
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<tr>
<td>Temperature Range</td>
<td>-40 to 85°C</td>
<td>-40 to 125°C (only grade 1)</td>
<td>-55 to 125°C (majority)</td>
<td>-55 to 125°C (majority)</td>
<td>-55 to 125°C</td>
<td>-55 to 125°C</td>
<td></td>
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<tr>
<td>100% 3 Temp Test</td>
<td>NO</td>
<td>NO</td>
<td>NO</td>
<td>YES</td>
<td>25, 125°C</td>
<td>YES</td>
<td>YES</td>
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<tr>
<td>Extra Qual/Process Monitors</td>
<td>NO</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
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<td>Life Test per lot</td>
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<td>NO</td>
<td>NO</td>
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<td>YES</td>
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</table>
Quality, Reliability, and the “Bathtub Curve”

Infant Mortality Hazard Function (decreasing with time)
Constant Hazard Function (random)
Wear-out Hazard Function (increases with time)
Bathtub Curve (sum of three hazard functions)

Bathtub Curve for advanced technology

“Useful lifetime”

https://www.samcointl.com/featured-solutions/failure-analysis/
A typical modern IC takes several dozen masks, each mask includes 10-20 steps => Finished product = 100 – 500 steps

Physical Sources of Variation

Process Average

[Diagram showing standard deviation limits and control limits]

Lower Control Limit
−6σ  −5σ  −4σ  −3σ  −2σ  −1σ  0  1σ  2σ  3σ  4σ  5σ  6σ

Upper Control Limit

99.7%

Light Source
Illumination Optics
Photomask
Projection optics
Aerial Image
Photosis
Wafer substrate

http://www.dcsc.tudelft.nl/~mverhaegen/n4ci/imwacol.htm


Multi-Fab Variability Example

• Fab-to-Fab
  – Usually worse than Lot-to-Lot
  – Fab equipment set / version
  – Fab layout / cycle time
  – Fab recipe / starting material
  – Fab metrology coverage
  – Fab controls / methods
  – Revisions / shrinks
  – Design sensitivity / component choice

• Lot-to-Lot
  – Usually worse than wafer-to-wafer
  – Process has a natural variation
  – Processes / Equipment drifts over time
  – Process tweaks to boost yield

Source: Texas instruments
COTS/Q100 Sourcing – Maximum Variability

COTS/Q100 Flow

- Wafer Fab EU
- Wafer Fab US
- Wafer Fab CH
- Wafer Fab JP
- A/T Site Malay
- A/T Site Thai
- A/T Site Taiwan
- A/T Site CH
- Material Set
- Material Set
- Material Set
- Material Set

Optimized for yield and supply stability (anonymity)
Commercial example: SN74HC138 3-Line To 8-Line Decoder

3 active wafer fabs
- TI SFAB in Sherman, Texas
- Subcontractor “A” in Taiwan
- Subcontractor “B” in China

3 assembly/test sites
- TI Mexico
- TI Taiwan
- Subcontractor “C” in Thailand

Each Fab/assembly/test site runs a similar but **NOT identical** baseline:
- Glassivation (protective overcoat)
- Base silicon wafers (vendor and doping spec)
- EPI versus non-EPI (doping profile/yield)
- Diffusion and metal profiles
- Process equipment
- Process recipes
- Process control limits
- Lead-frame source and geometries
- Mold compound (encapsulant)
- Mount compound (die attach)
- Wire bonder type and profile
- Wire type and other materials
- Injection mold press type / profile

Source: Texas instruments
Upscreening a Commercial/Q100 Product

- Full chip manufacturing and assembly variation
- Uncontrolled materials, die revisions, mixed lots, mixed fabs

COTS or Q100
Multiple lots, non-traceable
3 fab, 3 assembly sites

Qual, B/I, HTOL
"upscreening funnel"

Space Worthy?!
“My Momma says... **COTS** is like a box of chocolates... You never know what you're going to get.”
COTS/Q100 vs. Single Controlled Baseline

COTS/Q100 Flow

- Wafer Fab EU
- Wafer Fab US
- Wafer Fab CH
- Wafer Fab JP
- A/T Site Malay
- A/T Site Thai
- A/T Site Taiwan
- A/T Site CH
- Material Set
- Material Set
- Material Set
- Material Set

Optimized for yield and supply stability anonymity

SCB Lot Flow

- One Wafer Fab
- One A/T Site
- One Material Set

Traceability
Value of Single Controlled Baseline (SCB) Flow

- SCB greatly limits manufacturing variation
- Controlled manufacturing variation **CRUCIAL** to control rad effects

**Single Fab & Assembly site**

Single Controlled Baseline Lot
"SCB Lot Funnel"

Constrained variation

**Space Worthy!**

QUAL, B/I, HTOL
"Upscreening Funnel"
Less critical
Variation and the “Matryoshka Paradigm”

COTS Flow

Lot-to-Lot

Fab-to-Fab

A/T site-to-A/T site

SCB Lot Flow

Die-to-die

Wafer-to-wafer

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Real cost of using COTS

- High fail rate - only a bit more than a quarter have full mission success!!
- “Industrialist” (most successful) spend time/money up-screening BUT this does NOT seem to be enough.

Semiconductor Manufacturers are aware of the potential demand and are working on providing “intermediate-grades” that provide a good balance between price and space-grade-like performance…

M. Swartwout, “CubeSats and Mission Success: 2017 Update (with a closer look at the effect of process management on outcome),” NASA Electronics Parts and Packaging Program Electronics Technology Workshop, June 2017. (to 2016 excluding constellations)
TID-induced Isolation leakage MOSFETs


Parasitic n-channel is formed linking S-D at isolation edge in NMOS!!!

TID Variability: All about STI Morphology

- Morphology / uniformity
- Gate and Isolation thickness and quality
- Well, substrate, channel doping

Lot-to-Lot variation impact on HDR TID

<table>
<thead>
<tr>
<th>LM108</th>
<th>HDR</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lot 1</td>
<td>100</td>
<td>Pass</td>
</tr>
<tr>
<td>Lot 2</td>
<td>30</td>
<td>Pass</td>
</tr>
<tr>
<td>Lot 3</td>
<td>10</td>
<td>Fail</td>
</tr>
</tbody>
</table>

Source: Texas instruments

TID varies 10x over 3 lots!

Mitigation of SEL by Process

Substitute standard p substrate with highly-doped substrate w thin baseline EPI

from K. LaBel, et al., “Single event effect characteristics of CMOS devices employing various epi-layer thicknesses”, RADECs, Sept. 1995., pp. 258-262
Sources of Variability = Impact to SEL

Baseline device = high resistivity substrate. SEL lots = highly doped substrates with baseline EPI doping, 8 -10 um in thickness.

<table>
<thead>
<tr>
<th>Material</th>
<th>EPI thick. (um)</th>
<th>Temp.</th>
<th>SEL @ LET = 60</th>
<th>SEL @ LET = 85</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baseline</td>
<td>0.0</td>
<td>25°C</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Wafer A</td>
<td>8.0</td>
<td>25°C</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Wafer A</td>
<td>8.0</td>
<td>125°C</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Wafer B</td>
<td>9.0</td>
<td>25°C</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Wafer B</td>
<td>9.0</td>
<td>125°C</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Wafer C</td>
<td>9.5</td>
<td>25°C</td>
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</tr>
<tr>
<td>Wafer C</td>
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<tr>
<td>Wafer D</td>
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<td>25°C</td>
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<tr>
<td>Wafer D</td>
<td>10.0</td>
<td>125°C</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Fails SEL with a +0.5 um EPI thickness variation

Depending on average value of EPI thickness alone, normal EPI thickness variation could render some lots SEL sensitive!

- EPI thickness ± 4%
- EPI doping ± 15%
- Substrate doping ± 27%

Source: Texas instruments
Pros and Cons of COTS/COT+

“NASA wisdom says: use these parts very carefully, test extensively, and gather as much knowledge as possible.”

Reference NASA/TM-2014-218261

PROs
- Commercial availability
- Full assortment of functions
- Lots of me-too parts/pin replaceable
- Commercial pricing
- Plastic packaging
- No export restrictions

CONs
- Uncontrolled & maximal variation
- Need to be up-screened ($$$!)
  - Cost of test
  - Impact to cycle time
  - Impact if screen fails
- No traceability/obsolescence
- Plastic, Cu, Tin, etc.
- Voiding warranty/legal implications

“There are numerous data indicating that improper handling and testing of the parts can introduce more defects than are screened out.”

NASA PEM-INST-001
Summary

- COTS / COTS+ have been used successfully in some space missions.

- Manufacturing variation is one of the biggest risks of using COTS. Screening alone CANNOT always reduce risk to acceptable levels.

- We have demonstrated variation in TID and SEL performance large enough to cause mission failures given normal lot-to-lot manufacturing variation trends.

- Using grades that offer single controlled baseline lots is the surest way to minimize manufacturing variation by eliminating lot-to-lot, fab-to-fab, and A/T site-to-A/T site variation, GREATLY improving the efficacy of up-screening.

- Growing availability of alternate intermediate-grades may be the best solution, balancing risk, quality, and cost for many different types of missions.

- Manufacturers are responding to the growing demand for intermediate-grades. Volume demand at a reasonable price is needed to justify the development.
Thank you very much! Any Questions?