

# Robert C. Baumann

## Technology Leader / Consultant / Mentor - Semiconductor Industry

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- **Dynamic Leader:** Created and drove technology development teams in U.S. and Japan.
- **International Consultant:** Regularly resolved time-critical customer production issues.
- **Active mentor/Educator:** Driving international standards, export control policy (ITAR), university research projects, mentoring engineering groups and students.
- **Radiation Effects Expert:** Internationally-recognized, popular invited speaker.
- **31 Years of Experience:** Semiconductor technology, reliability, failure analysis.

**Fellow of the IEEE** (since 2005), **Texas Instruments Fellow** (2005, Emeritus in '16)  
**Distinguished Lecturer** (IEEE Electron Devices Society, 2006-2012)

Rice University, **Ph.D. Electrical Engineering**  
Bowdoin College, **B. A. Physics**, Cum Laude

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### Professional Experience

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**R&D Adjunct Professor, Lyle School of Engineering, SMU, Dallas TX** (10/18 – present)

- Developing characterization/simulation capabilities for reliability and radiation issues. Mentoring students on reliability and radiation effects in silicon and wide-band gap devices.
- Assisting in the creation of a research institute focused on mission-critical component and systems.

**President/Chief Consultant, Radiosity Solutions LLC, Dallas TX** (5/18 – present)

- Providing decisive advice, training, and solutions for reliability and radiation challenges for space products, satellite manufacturing, medical devices, and avionics.

**Chief Technologist, High Reliability Group, Texas Instruments, Dallas TX** (5/12 – 5/18)

- Guided cross-functional teams developing best-in-class space power products.
- Built in-house expertise in rad effects, removed reliance on 3<sup>rd</sup> parties, directly increased capability and customer confidence for higher sales and substantial annual cost savings.

**Technologist, Silicon Technology & Manufacturing, Texas Instruments, Dallas TX** (7/98 – 5/12)

- Created first on-line Soft Error Reliability Calculator. Directly contributed to major design-wins with hundreds of customers (Cisco, Apple, Nokia, Eriksson, etc.)
- Leader and primary coauthor of international radiation standards (JEDEC JESD-89, -89A, -221) and of SIA group that successfully challenged & changed ITAR export controls.

**Branch Manager, Reliability Sciences Group, Tsukuba R&D Center, Japan** (11/95 – 7/98)

- Reported to TI Japan President. Founded “special forces” team providing state-of-the-art failure analyses rapidly solving high-profile production issues for TI Japan product groups.

**Engineering Manager, ULSI Reliability Group, Texas Instruments, Mihomura, Japan** (7/93 – 11/95)

- Led reliability team driving successful DRAM/CPU development. Liaison for Japanese & U.S. groups.
- Invented novel stress circuit enabling 10x higher reliability (against CHC effects).

**Lead Engineer, DRAM Development Group, Texas Instruments, Dallas TX** (6/89 – 7/93)

- Discovered mechanism and solution leading to 10x improvement in electronics reliability, industry-wide (cosmic-ray neutron activation of <sup>10</sup>B in BPSG).
- Created oxide reliability models for 4 & 16 Mb DRAM burn-in reduction saving \$150M/year.
- Helped create/implement world-wide wafer-level reliability control (WLRC) methodologies.

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## Education

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- **1990 Rice U., Ph.D. Electrical Engineering**, “*Deposition, Characterization, & Applic. of Thin Film LiNbO<sub>3</sub>*”.
- **1986 VLSI Design Project, Rice University**, “*FFT Address Sequencer for Digital Signal Processing*”.
- **1984 Bowdoin College, B.A. Honors Physics (Cum Laude)**, “*Heat Capacity Measurements Using AC Microcalorimetry for Studying Phase Transitions in Gd and Liquid Crystals*”.
- **1983 Summer Internship (EIC Lab.)** – Optimized properties of WO<sub>3</sub> for variable transmittance windows.

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## Industry Leadership

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- **Primary author and Chairman** of committee (2000-2006) that **created JESD89 & JESD89A test standards**.
- **Chosen by B.o.D** to co-lead **SIA Experts Panel** (2000-2012) – drove negotiations with U.S. Government directly resulting in 2007 changes in ITAR that eliminated inadvertent export controls on all U.S. semiconductors.
- **Distinguished Lecturer** (2006-2012 – IEEE Electron Devices Society)
- **Vice-Chair for group** (2003-2010) developing alpha metrology standard **JESD221**.
- **2002-2004 IEEE IRPS, 2003 NSREC committee chairman**. IEEE Reviewer for various periodicals ('98-now).

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## Special Skills

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- **Native English** speaker, conversant in **French** and **Japanese**.
- **Proficient programmer** - Visual Studio 2015, VB6, etc. – developed several custom **radiation transport codes**.
- Designed and built several custom **high-vacuum** and **plasma and physical deposition systems**.
- Built and designed optics and systems for **Telescope, Foucault tester, and dark-field microscope**.
- Designed and built custom **analog and digital circuits** for **sound synthesis**.

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## Awards

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- **Fifteen Patents** (received TI's top patent incentive award).
- **2015 Outstanding paper** in NSREC Data workshop (one of 3 lead authors).
- **2013 NSREC Outstanding Conference Paper**
- **2011 IRPS Best Student Talk, 2009 IRPS Best Student Talk**
- **2006 JEDEC Chairman's Award** –(2006 for JESD89/89A - rarely given to individuals outside JEDEC)
- **Noel C. Little Prize** (1984) for outstanding work in experimental physics (Bowdoin College).

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## Recent Publications/Presentations (> 100 papers, 49 invited, 1 handbook, 2 book chapters, 15 patents)

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- Main author, "**TI's Radiation Handbook for Electronics**", released online and published, July 2019.
- Invited Short Course, “**Radiation Hardness Assurance in the "Wild West" of Commercial Space**”, *57<sup>th</sup> International Nuclear and Space Radiation Effects Conf. (NSREC)*, IEEE, Virtual Conference, Dec. 2020.
- Invited short-course, “**From COTS To Space Grade Electronics: Which Is The Best For Your Mission?**”, European Conf. on Radiation and its Effects on Components and Systems (RADECS), Göteborg, Sweden, Sept. 17, 2018.
- M. Hamlyn et al., “**Transmission Line Pulse Test Method for Estimating SEB Performance of n-Channel Lateral DMOS Power Transistors**”, *IEEE Trans. Nuc. Sci.*, 65(1), Jan. 2018, pp. 249-255.
- Invited plenary, “**Funny stories from terrestrial radiation effects**”, *European Conf. on Rad. and its Effects on Components and Systems (RADECS)*, Geneva, Oct. 2017.
- Invited plenary, “**The Natural Radiation Environment and its Impact in Microelectronics (for non-device experts)**”, *40<sup>th</sup> Annual International Meeting on Radiation Processing (IMRP)*, Vancouver, BC, Nov. 2016.
- Invited plenary, “**Silicon Amnesia and Dementia: Radiation Effects in Microelectronics**”, *Council on Ionizing Radiation Measurements and Standards Conference (CIRMS)*, NIST, Gaithersburg, MD, April 2015.
- Invited Short Course, “**Landmarks In Terrestrial Single-Event Effects**”, *50<sup>th</sup> International Nuclear and Space Radiation Effects Conf. (NSREC)*, IEEE, San Francisco, CA, July 2013.